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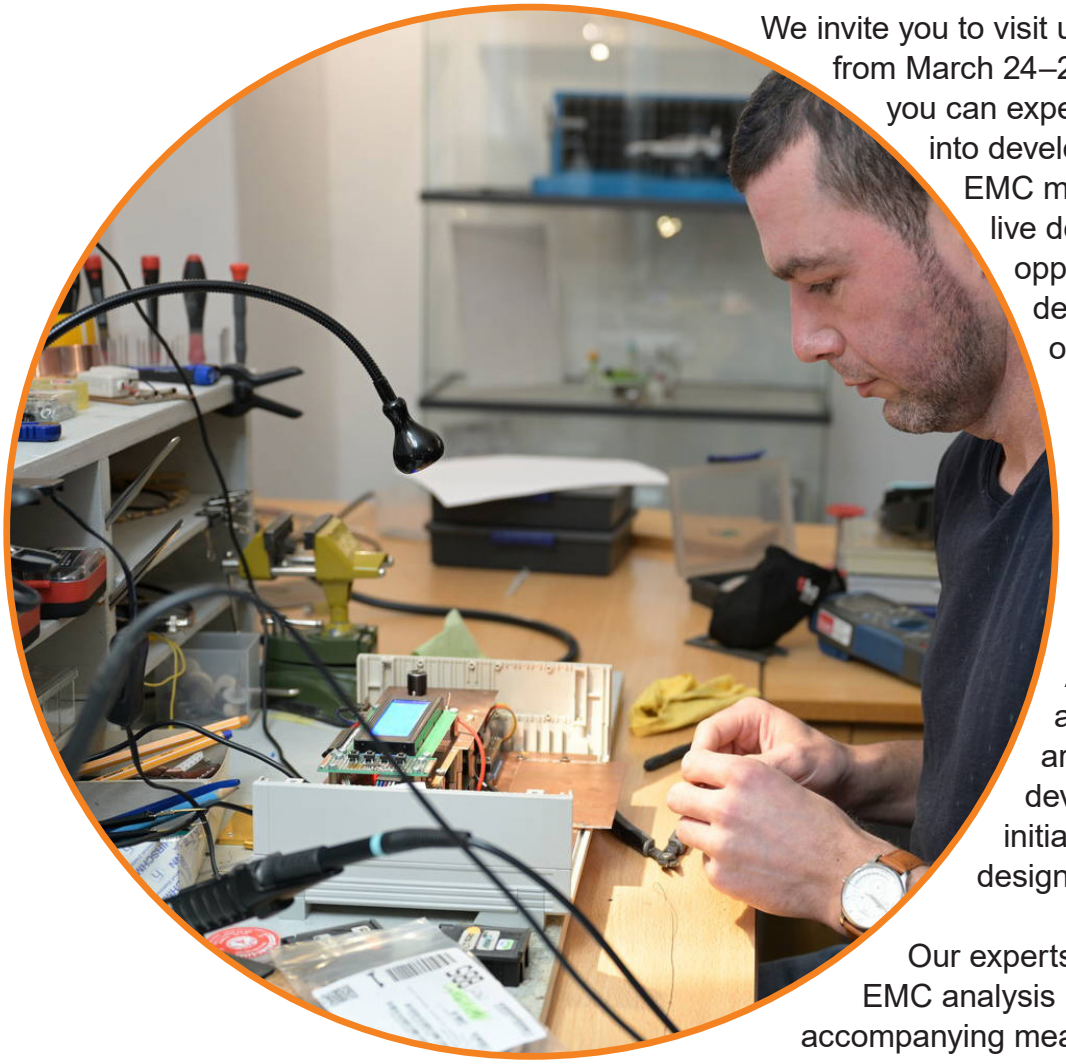
EMV Cologne 2026

in Cologne – Germany



We invite you to visit us at EMV 2026 in Cologne from March 24–26, 2026. At our booth, you can expect practical insights into development-accompanying EMC measurement technology, live demonstrations, and the opportunity to have your device under test analyzed on site by our experts.

Weakness analyses for your electronics

Bring your PCB assembly or device and book a slot for a measurement-based analysis at our booth! Are you currently facing an EMC problem? Or are you working on a new development and need an initial assessment of your design?

Our experts will perform a free on-site EMC analysis using our development-accompanying measurement technology—covering both emissions and immunity. You'll receive concrete development impulses, indications of weak points, troubleshooting tips, and recommendations for possible design optimizations.

To sign up, please email us with a brief description of your electronics and your preferred measurement day at sales@langer-emv.de.

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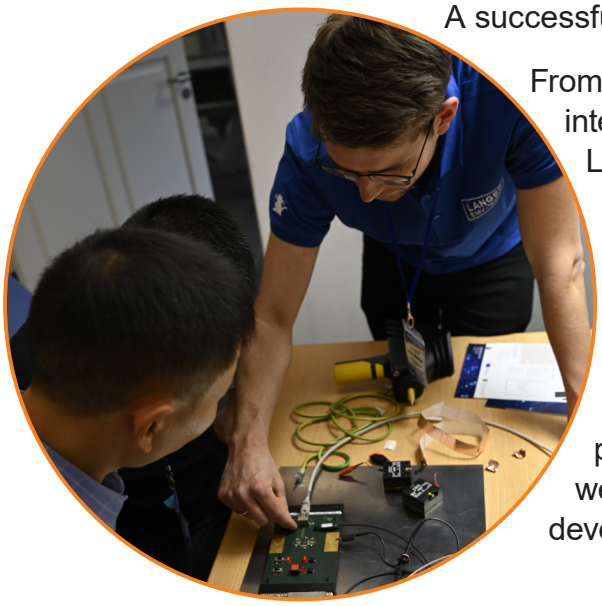
Distributor Week

in Bannewitz – Germany



A successful Distributor Week 2025 is behind us!

From November 10 to 14, numerous representatives of our international partners and distributors were on site at Langer EMV-Technik GmbH:

ATS Technology Ltd., Datatec, Noise Tech Co., Ltd., Rohde & Schwarz, TestEquity GmbH, Zhejiang Noyetec Technology, CDIL Group, Peking Xinghe Yihai Technology, JS Toyo, H TEST und X-Test.

Hands-on workshops and open discussions included product trainings and technical exchange. Together, we deepened applications, shared experiences, and developed ideas for future projects.

Many thanks to all participants for the productive collaboration and open dialogue! We look forward to the upcoming event in 2026 and to welcoming just as many participants again.

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EMC Experimental Seminars

EMC Experimental Seminars Dates 2026

Immunity ***Basics & Troubleshooting*** *3 days*		***Emission*** ***Basics & Troubleshooting*** *3 days*	
April - German	**14. - 16.**	**April- German**	**21. - 23.**
May - English	**19. - 21.**	**May - English**	**05. - 07.**
June - German	**09. - 11.**	**June - German**	**16. - 18.**
September - German	**15. - 17.**	**September - German**	**22. - 24.**
October - German	**06. - 08.**	**October - German**	**27. - 29.**
November - German	**24. - 26.**	**December - German**	**01. - 03.**

- Course materials and catering for participants are included.
- Location: Rosentitzer Straße 73, 01728 Bannewitz (near Dresden), Germany.

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PT4 set

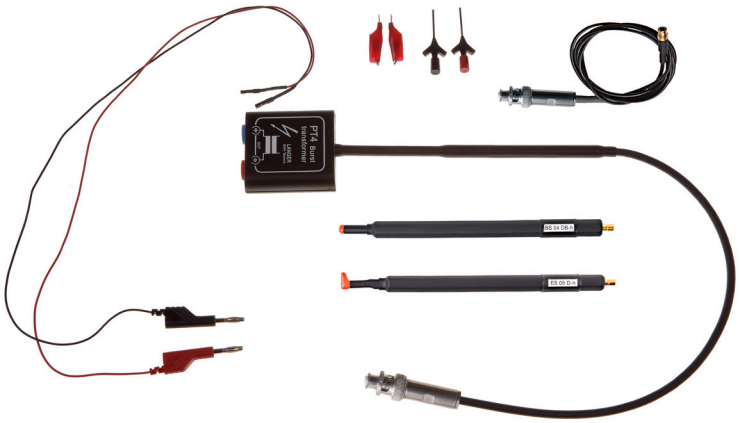
EFT Generator Set

The PT4 set is used to analyze immunity of assemblies and devices efficiently. The PT4 burst transformer converts the pulses of the EFT/burst generator into potential free burst pulses. These are injected into individual sections of the device under test, enabling the developer to locate its susceptible areas.

The set includes a magnetic and an electric field source which are also supplied by the EFT/burst generator. The field, which emerges from the head of the field source, is used to scan the surface of the device under test. This allows the weak spots to be located with precision and assigned to the fault patterns that occur in compliance tests.

The burst transformer and the connecting cable come with either an SHV plug (HV SHV-SMB 1 m) or a Fischer plug (HV FI-SMB 1 m). Please select the desired connector/plug when ordering.

Measurements taken with an oscilloscope during interfence are possible because the pulses from the burst generator are galvanically isolated. This allows for a significant reduction in faulty measurements despite possible interference.



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EMC Immunity of Devices

Interference suppression of an electronic device with burst transformer and field sources

The requirements for modern electronic devices are high.

These include, for example:

- high immunity to interference,
- an optimized, preferably small shielded enclosure, and
- low power consumption.

What approaches and tools can support developers in this work?

This article presents an interference suppression strategy that helps developers eliminate interference in the device and further harden it when the interference patterns are known.

In the planning phase of a new development, evaluating the implemented EMC measures is difficult for the developer. The EMC characteristics of the selected circuits are not known or only partially known. If the developer receives more precise EMC parameters for the circuits that are planned for use in the design, the EMC-related decisions become more reliable. Obtaining these parameters is no longer a problem today with specialized IC measurement technology. If the planned production volume of the device does not justify the cost of dedicated IC testing, then a development-accompanying investigation of potential susceptibility points in the prototype device is the classical approach.

The varying EMC experience and accumulated insights of the developer when working with prototypes influence the risk of failing the standard immunity test. If this happens, the device under test must be reworked.

To achieve the goal of high immunity, the developer deploys various countermeasures in the electronics. Effective EMC measures are only successful when they can be derived from concrete knowledge about the coupling paths. Since each newly developed electronic assembly includes the risk of incorrect assumptions, it is necessary to experimentally evaluate the immunity of the device.

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For effective pre-compliance EFT/Burst investigations on the electronic device, the interaction of the EFT/Burst generator with field sources and burst transformers has proven successful. The practical strategy for investigations of the assembly—aimed at clarifying interference phenomena that are difficult to analyze—will be presented here.

The insights gained from this can be used to derive targeted EMC measures to optimize the electronic device. Using the same tools, the implemented EMC measures can be evaluated for their effectiveness.

This systematic and goal-oriented approach can lead to significant time and cost savings during the development of an device.

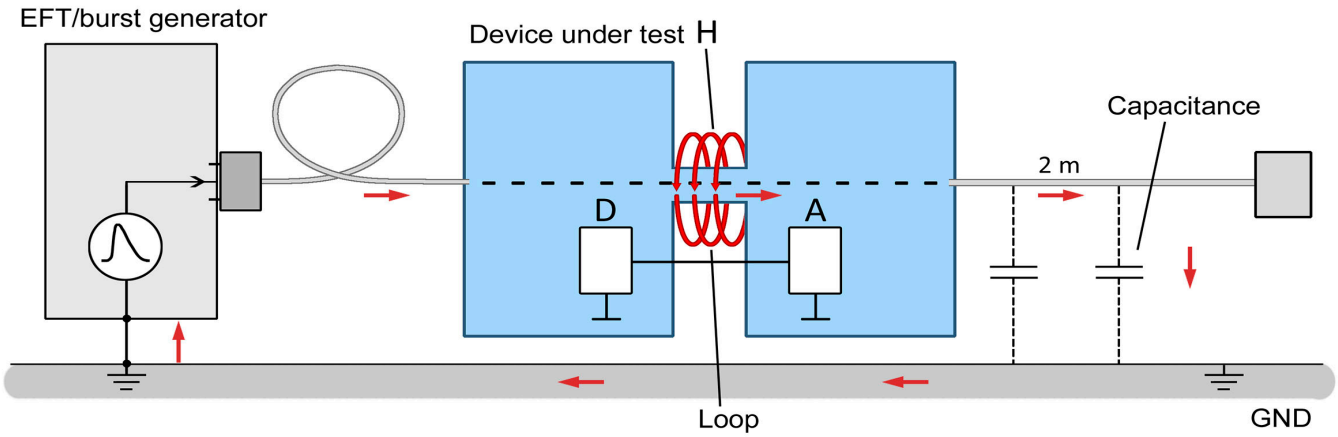

Figure 1: Standard test of an electronic device

Preparation: Setting up an electronic device for testing according to the IEC 61000-4-4 device standard (Figure. 1)

The device under test (DUT) is positioned at a distance of 10 cm above a reference ground plane. The disturbance current loop is closed through the output of the EFT/Burst generator (hereinafter referred to as the generator), the DUT's power supply, and the parasitic capacitance of connected cables to the ground plane, and from there back to the generator via a ground connection (Figure 1). The disturbance current flowing through the DUT generates magnetic fields inside the DUT. These magnetic fields couple into trace networks and induce interference voltages, thereby disturbing the circuitry of the DUT.

The voltage of the generator is applied between the DUT and the reference ground plane. This voltage generates electric fields that extend from the DUT to the reference ground plane. These electric fields can likewise act on traces and components of the DUT—for example, crystal oscillators, reset lines, bus systems, and so on. Through this mechanism, the electric fields can also disturb the DUT's circuitry.

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If a cable is connected as shown in Figure 1, the additional capacitive currents amplify the magnetic fields on the device. Whether the capacitive or inductive disturbance path is responsible for the observed malfunction depends on the characteristics of the DUT. The following describes the procedure for interference suppression of the device.

Step one: Type testing of the DUT in the laboratory according to IEC 61000-4-4

The DUT is wired as shown in Figure 1. The disturbance event generates electric and magnetic fields at the DUT. These can disturb the DUT through its trace networks and components. The disturbances manifest as functional errors. In the setup shown in Figure 1, this may be a failure of the analog circuits. Based on the measurement principle and the resulting error pattern, it is not possible to determine which specific part (trace network and associated IC) is being disturbed or whether magnetic or electric fields are causing the interference. Clarification and narrowing down of the fault follow in subsequent suppression steps.

Step two: Using a Burst Transformer as an Accessory for EFT/Burst Generators According to IEC 61000-4-4 for Fault Localization

With the setup in Figure 1, it is difficult to further localize the fault on the circuit. The reason is that the generator always operates with reference to ground, and the reference ground plane must always be the injection point. It is not possible to selectively inject two-pole into specific areas of the DUT to narrow down the fault.

To selectively inject two-pole into the DUT, potential-free, differential generator outputs are required. The ground-referenced output of the generator can be converted into a two-pole, potential-free, differential output using a burst transformer (hereinafter referred to as the transformer).

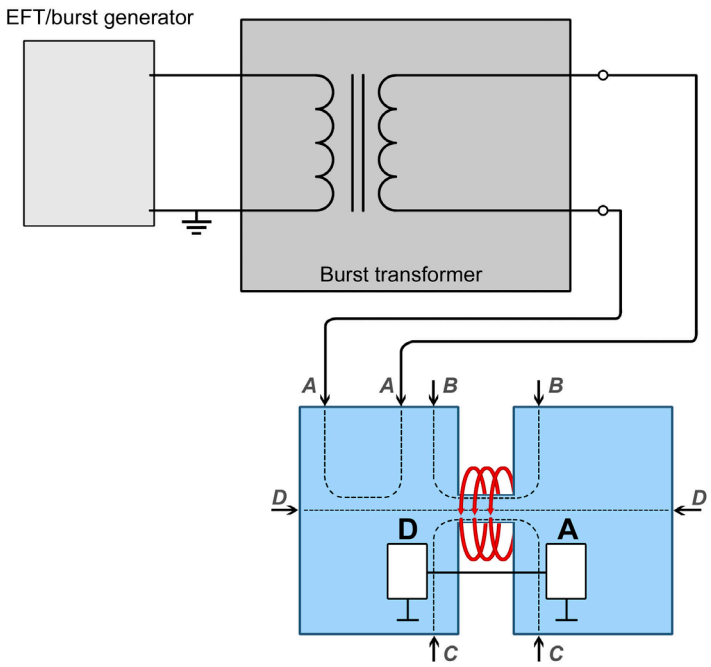

Figure 2: Selective potential-free feeding of EFT/burst interference current into defined module parts to roughly limit the range of the interference sink

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In Figure 2, the basic circuit diagram of such a transformer is shown. With the two-pole output of the transformer, it is possible to inject into the ground system of the DUT. Figure 2 illustrates how injection into the DUT can be performed at various points from AA to DD. Figure 3 shows a corresponding test setup using a burst transformer.

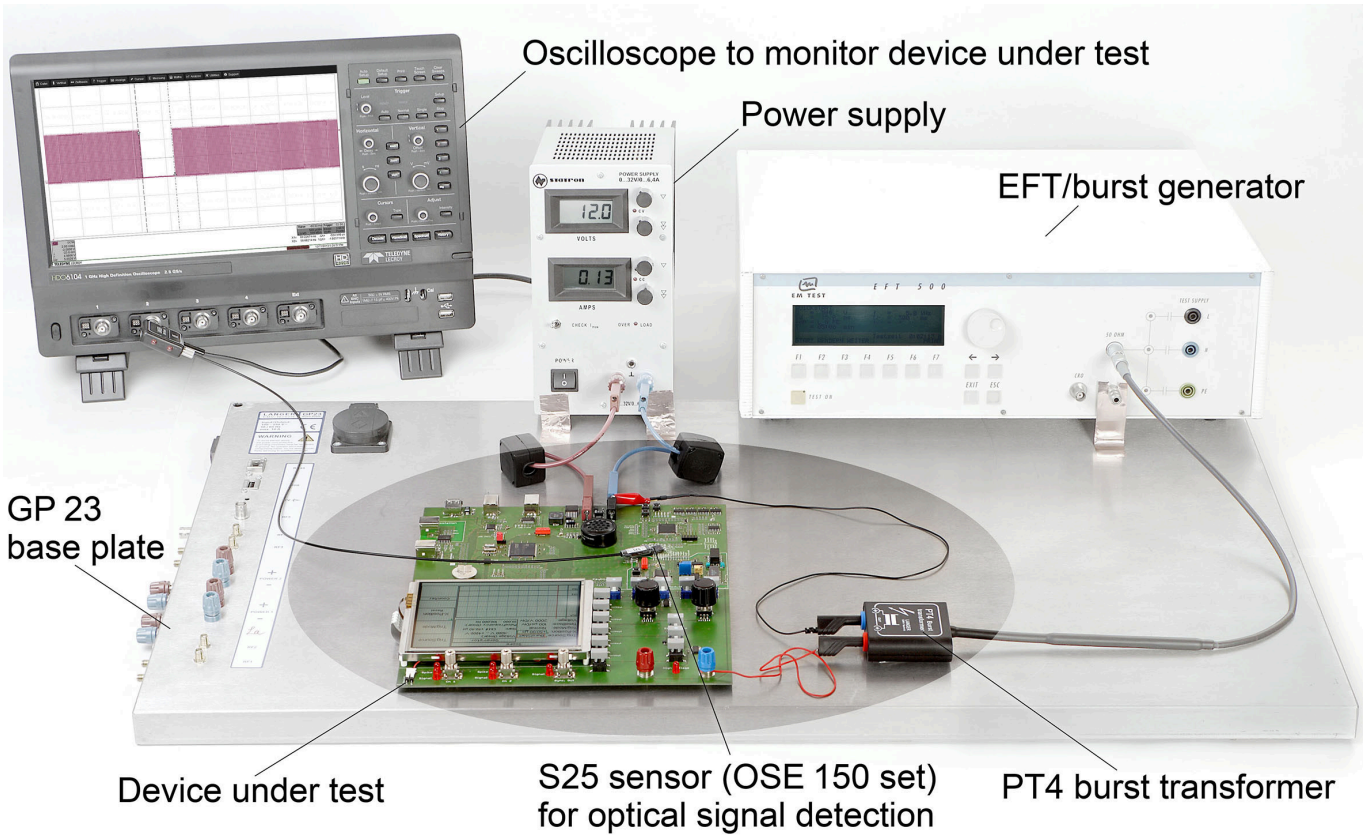

Figure 3: Test set-up with burst transformer

It is anticipated that a disturbance sink exists in the DUT that reacts to magnetic fields. This disturbance sink is assumed to be a trace connection between the digital and analog circuit areas. The ground planes of the digital and analog circuit areas are typically separated by a gap in the layout and connected at a single point near the most sensitive component. Traces that run from the analog to the digital section may be routed across this gap. As a result, a loop is formed between the ground system, the single-point connection, and the trace, as visible in Figure 1. When the disturbance current (Figure 1) flows through the single-point connection, its magnetic field penetrates this loop. The magnetic field generated by the disturbance current induces an interference voltage in the loop, which can disturb a connected analog IC, for example.

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From this situation, a generally valid suppression strategy for magnetic-field-related interference can be derived. When the outputs of the transformer are connected at points AA, hardly any disturbance current flows through the single-point connection, and the analog IC is not disturbed. This means that no disturbance sink exists in the AA area of the device. When the outputs are connected at DD, the error pattern appears as in the type test (Figure 1).

When the transformer is connected at BB, the error pattern appears because the disturbance sink is affected. The influence will not be as strong as when the transformer is connected at CC. At CC, the highest level of influence occurs. By examining the layout in the CAD system, the gap can be identified as a weak point at this location. At this stage, it is not yet known which trace and which IC input are affected.

Step three: Localizing the Disturbance Sink Using Field Sources

The field sources are connected to the HV output of the generator and supplied with EFT/Burst. There are field sources that generate magnetic fields (H-field source) as well as field sources that generate electric fields (E-field source). Since we are dealing with a disturbance sink sensitive to magnetic fields, a field source that generates magnetic fields must be selected for further investigation. The field source should produce a relatively narrow field beam at its tip so that the location of the disturbance sink can be resolved accurately.

The field source is guided at a small distance above the surface of the DUT (Figure 4). When the trace belonging to the disturbance sink is approached, an influence will occur. Therefore, the generator level must be reduced so that the influence occurs only in the immediate vicinity of the trace. A similar effect can be achieved by increasing the distance between the field source and the DUT surface. However, increasing this distance reduces the resolution of the field source.

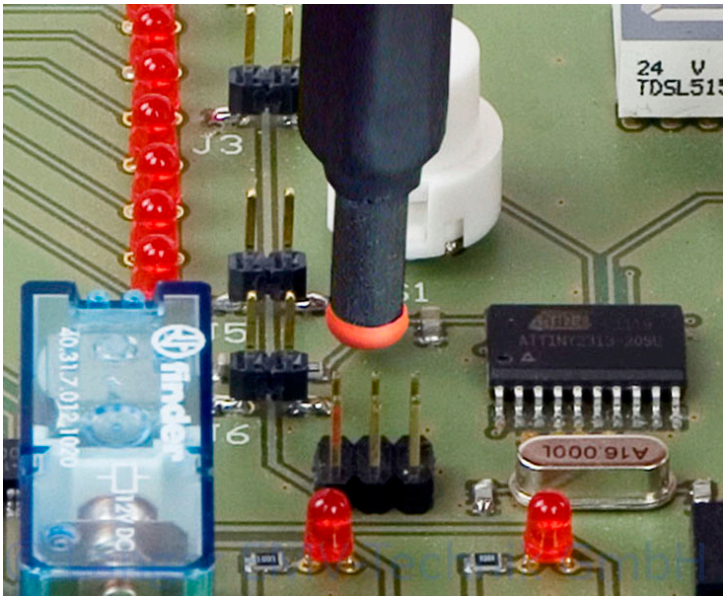

Figure 4: Application of a field source above the DUT

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The influence is strongest when the probe is guided into the interior of the loop (see the loop visible in Figure 1). The boundary of the loop at the gap can be located relatively accurately using the field source. From this localization, the trace responsible for the disturbance can be identified in the layout. However, if the traces are densely packed, the responsible trace cannot be precisely located. In such cases, two or three traces may be suspected. A more precise narrowing can be estimated based on the function of the traces. In the layout, the traces must be followed to the corresponding IC. Based on the signal assignment, potential sensitivities can then be inferred. If this is not possible, the traces should be followed in the layout until a point is found where one of the traces runs individually. At this point, the trace can be selectively tested with the H-field source. Afterwards, countermeasures such as filters at the IC inputs or closing the gap with ground can be used to test whether the functional error has been eliminated.

Step four: Localizing E-Field-Sensitive Disturbance Sinks

In addition to the disturbance sink sensitive to magnetic fields, E-field-sensitive disturbance sinks may also be present. These disturbance sinks generally cannot be detected using steps 2 and 3, because the transformer connection in step two generates mainly magnetic fields in the DUT and does not produce significant voltage differences. To generate voltage differences, the transformer must be connected to the DUT in a single-ended manner. The other pole can be connected to the reference ground plane as in step one. It is advantageous to decouple all of the DUT's line connections using multiple ferrite cores so that disturbance current flow through parasitic capacitances is suppressed. This prevents the DUT from being disturbed by magnetic fields. If errors occur, it is proven that they are very likely caused by electric fields. However, E-field-sensitive disturbance sinks cannot be directly localized using this method.

By bringing a hand close to the DUT, the fields at the surface can be intensified, thereby triggering E-field-sensitive disturbance sinks. The effect of hand proximity can be supported by adjusting the voltage level of the generator. The spatial resolution of the disturbance sink is usually not very high, but this approach can still lead to a usable result.

Using a large-area E-field source connected to the second pole of the transformer (for this, the second pole must be disconnected from the reference ground plane) can improve the localization in a manner similar to the hand-proximity method. A 5 × 5 cm metal plate connected to the second pole of the transformer can serve as an E-field source. Metal plates of different sizes may be used for localization. The field source should be guided using an insulating rod. With this method, the disturbance sink can typically only be localized roughly.

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To precisely locate the disturbance sink, higher resolution is required. For this purpose, special E-field sources are used, connected to the HV output of the generator. To achieve the necessary resolution, the E-field sources must have a field electrode at the tip in the millimeter range. The electrode is connected to the coaxial inner conductor of the HV cable. Since the disturbance sink has already been roughly localized, the field source can be placed specifically on traces or components, IC pins, and so forth.

The field source must be appropriately insulated to prevent flashovers into trace networks and to avoid damage. If functional errors occur when the E-field source is applied, the trace or component is identified as the disturbance sink. The trace itself is usually not the direct problem; rather, the component connected to the trace (IC, transistor, reference source, etc.) is responsible. Based on the type of component connection and its associated function, suitable countermeasures (filters, shielding) can be derived. These measures are implemented and verified using tests with the transformer and the field sources.

Conclusion

When a sufficient number of disturbance sinks has been eliminated, it is advisable to perform a type test according to Step 1 to verify whether the achieved hardening of the DUT is adequate. For practical application, the following should be taken into account: Step 1 is generally always performed first. Whether Step 2, the magnetic-field suppression, or Step 4, the electric-field suppression, should follow cannot be predicted with certainty. If, during the type test, for example, a hand-proximity test is performed and the DUT exhibits corresponding reactions, this indicates E-field sensitivity, so that one can proceed directly with Step 4, the electric-field suppression.

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Nöthnitzer Hang 31
01728 Bannewitz
Germany